

REMARKS

Claims 1, 2 and 6 have been amended. Claims 1-12 remain for further consideration. No new matter has been added.

The objections and rejections shall be taken up in the order presented in the Official Action.

Claims 1, 2 and 6 have been amended to obviate the objections.

1-2. Claim 1 currently stands rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in U.S. Patent 5,043,782 to Avery (hereinafter "Avery") and Japanese Patent Application JP361292351A to Wada et al (hereinafter "Wada").

Claim 1 recites an electrostatic discharge protective structure arranged to protect an integrated circuit connected between a first voltage bus having a first supply voltage (VCC) and a second voltage bus having a second supply voltage (VSS). The protective structure includes:

"a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally designed bipolar transistors (T1-T3)." (cl. 1)

Significantly, the protective device of claim 1 includes a single track resistor that precedes each of the control connections of the bipolar transistors.

A. A Prima Facie Case of Obviousness Has Not Been Presented

After admitting that Avery does not teach a single-track resistor to precede every control connection in order to enable a large input surge voltage to be more uniformly dispersed, the Official Action then contends that Wada teaches the application of one track resistor (see Official Action, pg. 4). The Official Action then abruptly concludes *"it would have been obvious to one of ordinary skill in the art to modify the invention by Avery at the time it was made so as to include the stipulation that a single-track resistor be included as stipulated in claim 1 of Applicants."* (Official Action, pg. 4).

"Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination." In re Geiger, 2 U.S.P.Q.2d 1276, 1278 (Fed. Cir. 1987). "Although the Commissioner suggests that [the structure in the primary prior art reference] could readily be modified to form the [claimed] structure, '[t]he mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification.'" In re Laskowski, 10 U.S.P.Q.2d 1397, 1398 (Fed. Cir. 1989), citing In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984). In addition, "[w]hen the incentive to combine the teachings of the references is not readily apparent, it is the duty of the examiner to explain why the combination of the reference teachings is proper." Ex parte Stone, 2 U.S.P.Q.2d 1788, 1790 (Bd.App. & Int'f 1986) (emphasis added).

The Official Action is void of any reasoning of why one of ordinary skill would have modified Avery. As noted above, it is fundamental that obviousness can not be established absent some teaching to combine the references, or a suggestion or incentive supporting the combination of references. See In re Gieger, at 1278 (Fed. Cir. 1987). Hence, a prima facie case of obviousness has not been presented since there is no proper teaching, suggestion or incentive of record in the Official Action that would lead one of ordinary skill in the art to modify Avery as suggested. Specifically, noticeably missing from the Official Action is the necessary cite to the teaching or suggestion in the prior art references as to why someone would combine Avery and Wada in the manner suggested in the Official Action.

B. There is no Proper Combination of References Which Disclose the Invention Set Forth in Claim 1

Assuming for the moment, without admitting, that Avery and Wada are properly combinable, then modifying Avery based upon the teaching of Wade still fails to render claim 1 obvious. As set forth above, Avery does not disclose (nor suggest) a protective device having a plurality of transistors, wherein a single track resistor precedes a control connection on each of the plurality of transistors.

Wada discloses that the channel length L of the transistor is gradually reduced to gradually decrease a breakdown voltage BV_{DS} between the source and the drain. As a result, an input surge voltage can be uniformly dispersed in the channel of the transistor. Significantly, in Wada, the resistor 1 does not cause the current to be uniformly distributed to the protecting MIS

transistors 4. Varying the channel length L for each of the transistor 4 as shown in FIG. 1 of Wada is what causes the uniform current flow.

One of ordinary skill in the art would not look to Wada, since Wada discloses varying the channel length. As set forth in Avery, a shorter channel length transistor QS is used to drive a longer channel length structure QL into conduction. If the long channel length of the transistors QL were modified to include channel lengths of various sizes, then the circuit of Avery may no longer operate for its intended purpose. Avery expressly discloses a system design that employs the shorter channel length transistor QS that is used to drive the longer length channel structure transistor QL into conduction. If the channel length of transistors QL are gradually decreased, then Avery may no longer conduct properly and snap back. Therefore, a skilled person would not modify the selected long channel lengths of Avery to include the gradual reduced channel lengths disclosed in Wada.

In addition, modifying Avery according to the Mata may result in an operable device.

3. Claims 2-5 currently stand rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Wada and U.S. Patent 5,075,271 to Smith (hereinafter "Smith").

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above.

4. Claims 2-5 currently stand rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Wada, Smith and U.S. Patent 5,623,387 to Li et al (hereinafter "Li").

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above.

5. Claims 7-12 currently stand rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Wada, Smith, Li and U.S. Patent 6,277,689 to Wong et al (hereinafter "Wong").

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above.

For all the foregoing reasons, reconsideration and allowance of claims 1-12 is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Micronas.6247
09/852,123

Respectfully submitted,

A handwritten signature in cursive script, reading "Patrick O'Shea". The signature is written in dark ink and is positioned above a horizontal line.

Patrick J. O'Shea

Reg. No. 35,305

Samuels, Gauthier & Stevens, LLP

225 Franklin Street, Suite 3300

Boston, MA 02110

(617) 426-9180, Ext. 121

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 5 with the following rewritten paragraph:

----This application contains subject matter related to co-pending application designated serial number ~~xx/xxx,xxx~~ 09/852,123, filed May 8, 2001 and entitled Electrostatic Discharge Protective Structure.--

IN THE CLAIMS:

Amend claim 1 and add claims 13-14 as follows:

- 1 1.(amended) An electrostatic discharge (ESD) protective structure that protects an integrated
- 2 circuit connected between a first voltage bus with a first supply voltage (VCC) and a second
- 3 voltage bus with a second supply voltage (VSS), said electrostatic discharge protective structure
- 4 comprising:
- 5 a plurality of laterally designed bipolar transistors each having a first load line connected
- 6 to the first voltage bus and a second load line connected to the second voltage bus, wherein said
- 7 first load lines are electrically parallel and said second load lines are electrically parallel to one

8 another, each of said laterally designed bipolar transistors includes a control connection
9 connected to one of the voltage buses;
10 a single track resistor (RB) co-integrated into a semiconductor body, wherein said single
11 track resistor precedes every control connection (B) of said laterally designed bipolar transistors
12 (T1-T3).

1 2.(amended) The electrostatic discharge protective structure of claim 1, wherein said
2 semiconductor body has embedded therein at least one emitter zone and at least one collector
3 zone of the first conduction type and at least one base zone of the second, opposite conduction
4 type, wherein a well-shaped region is inserted into said semiconductor body between said zones
5 of the first conduction type and said base zone or said base zones, so as to extend the effective
6 mean free path of the charge carriers to said base zone.

1 6.(amended) The electrostatic discharge protective structure of claim 5, wherein said base
2 zones laterally enclose said emitter zones ~~at~~ and said collector zones.